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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,237	03/29/2006	Wolfgang Kemper	DE03 0231 US1	3782

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EXAMINER	
SITTON, NELSON	

ART UNIT	PAPER NUMBER
4158	

NOTIFICATION DATE	DELIVERY MODE
12/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/562,237	KEMPER, WOLFGANG	
	Examiner	Art Unit	
	NELSON SITTON	4158	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *22 Dec 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.

(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.

(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Appropriate correction is required.

4. The disclosure is objected to because of the following informalities:

Page 6, line 1: "The protection circuit shown in Fig. 1" should read -- The protection circuit shown in Fig. 2.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 6-8 are rejected under 35 U.S.C 103(a) as being unpatentable over Krakauer et al. (US Patent No. 5,617,283 and Krakauer hereinafter) in view of Ker et al. (US Pub No. 2002/0050615 A1 and Ker hereinafter).

Krakauer discloses an integrated protection circuit for integrated circuit device comprising:

a first transistor whose control outputs are connected between a pad and a control input of a clamping device [claim 1] (45a or first transistor, 18 or clamping device, Fig. 2; col. 4, lines 30-31);

control outputs of said clamping device being connected between said pads and a reference voltage terminal [claim 1] (12 or pad, 18 or clamping device, Fig. 2; col. 4, lines 42-44);

a second transistor, whose control outputs are connected between the control output of said first transistor and said reference voltage terminal [claim 1] (45b or 2ND transistor, Fig. 2; col. 4, line 49);

The protection circuit, where the first transistor is a p-channel MOS transistor [claim 6] (45a, Fig. 2);

The protection circuit, where the second, third and fourth transistor are n-channel MOS transistors [claim 7] (18, Fig. 2);

The protection circuit, where the clamping device is a n-channel MOS transistor laid out for ESD protection [claim 8] (18, Fig. 2; col. 42-44);

Krakauer did not expressly disclose:

time-delay means connected between a supply voltage terminal and said control inputs of said first transistor and said second transistor [claim 1]

The protection circuit, where the time-delay element comprises a series connection of a resistor and a capacitance [claim3];

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Krakauer, as evidenced by Ker.

Ker discloses a low voltage triggered electrostatic discharge protection device and relevant circuitry having:

time-delay means connected between a supply voltage terminal and said control inputs of said first transistor and said second transistor [claim 1] (86, Fig. 6b; paragraph 0037, lines 17-18; paragraph 0038, lines 17-18) to provide time delay means to the protection circuit;

The protection circuit, where the time-delay element comprises a series connection of a resistor and a capacitance [claim3] (86, Fig.6b; paragraph 0037, lines 17-18)

Giving the teaching of Ker, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Krakauer by employing the well known or conventional features of designing an ESD protection device having a quick turn-on speed and superior ESD tolerance, such as disclosed by Ker, in order to improve the low voltage triggered electrostatic discharge protection device and its applications.

7. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US Patent No. 5,617,283 and Krakauer hereinafter) in view of Ker as applied to claim 1 above, and further in view of Lai et al. (US Pub. No. 2003/0235022 A1 and Lai hereinafter).

Although the method and apparatus disclosed by Krakauer in view of Ker shows substantial features of the claimed invention (discussed in the paragraph above), it fails to disclose:

The protection circuit, where the pad is a signal pad or a power supply pad [claim 2];

The protection circuit, where a diode is connected between the pad and the supply voltage terminal [claim 11];

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Krakauer in view of Ker, as evidenced by Lai.

Lai discloses a gate equivalent potential circuit and method for I/O ESD protection having:

The protection circuit, where the pad is a signal pad or a power supply pad [claim 2] (40, Fig. 4A; paragraph 0021, line 6) to provide a I/O or power supply pad to the protection circuit;

The protection circuit, where a diode is connected between the pad and the supply voltage terminal [claim 11] (Fig. 4a, paragraph 0021, lines 3-4) to provide a diode to the protection circuit.

Giving the teaching of Lai, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Krakauer in view of Ker by employing the well known or conventional features of ESD protection for a gated equivalent potential integrated circuit (IC) and method, such as

disclosed by Lai, in order to have the used and unused equivalent potential during an ESD event.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US Patent No. 5,617,283 and Krakauer hereinafter) in view of Ker et al. (US Pub. No. 2002/0050615 A1 and Ker hereinafter) as applied to claim 3 above, and further in view of Yu et al. (US Patent No. 6,031,405 and Yu hereinafter).

Although the method and apparatus disclosed by Krakauer in view of Ker show substantial features of the claimed invention (discussed in the paragraph above), they fail to disclose:

The protection circuit, where the time-delay element comprises a third transistor, the resistor being connected between the supply voltage terminal and said third transistor, said third transistor forming the capacitance [claim 4]

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Krakauer in view of Ker, as evidenced by Yu.

Yu discloses an ESD circuit immune to latch-up during normal operation having:

The protection circuit, where the time-delay element comprises a third transistor, the resistor being connected between the supply voltage terminal and said third transistor, said third transistor forming the capacitance [claim 4] (Fig. 4; col. 3, lines 4-5; col. 4, lines 36-39) to provide a time delay element to the protection circuit;

Giving the teaching of Yu, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Krakaeur in view of Ker by employing the well known or conventional features of ESD protection circuit, such as disclosed by Yu, in order to prevent the occurrence of latch-up even if noise interference happens during normal operation.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US Patent No. 5,617,283 and Krakauer hereinafter) in view of Ker et al. (US Pub No. 2002/0050615 A1 and Ker hereinafter) and Yu et al. (US Patent No. 6,031,405 and Yu hereinafter) as applied to claim 4 above, and further in view of Ulmer (US Patent No. 4,612,497 and Yu hereinafter).

Although the method and apparatus disclosed by Krakauer in view of Ker and Yu show substantial features of the claimed invention (discussed in the paragraph above), they fail to disclose:

The protection circuit, where a fourth transistor is provided whose control outputs are connected between the reference voltage terminal and the control output of the third transistor and whose control input is connected to said reference voltage terminal [claim 5]

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Krakauer in view of Ker and Yu, as evidenced by Ulmer.

Ulmer discloses a MOS current limiting output circuit having:

The protection circuit, where a fourth transistor is provided whose control outputs are connected between the reference voltage terminal and the control output of the third transistor and whose control input is connected to said reference voltage terminal [claim 5] (46, 48, Fig. 2; col. 3, lines 44-47) to provide transistors (third and fourth) to the protection circuit;

Giving the teaching of Ulmer, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Krakaeur in view of Ker and Yu by employing the well known or conventional features of CMOS current limiter circuit having a non-complex structure, such as disclosed by Ulmer, in order to provide accurate current limiting protection.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US Patent No. 5,617,283 and Krakauer hereinafter) in view of Ker et al. (US Pub. No. 2002/0050615 A1 and Ker'615 hereinafter) as applied to claim 1 above, and further in view of Ker et al (US Patent No. 6,912,109 B1 and Ker'109 hereinafter).

Although the method and apparatus disclosed by Krakauer in view of Ker'615 shows substantial features of the claimed invention (discussed in the paragraph above), it fails to disclose:

The protection circuit, where the clamping device is a parasitic npn transistor [claim 9].

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Krakauer in view of Ker'615, as evidenced by Ker'109.

Ker'109 discloses power rail EDS clamp circuits with well triggered PMOS having:

The protection circuit, where the clamping device is a parasitic npn transistor [claim 9] (Fig. 4; col. 5, lines 35-42) to provide a parasitic npn transistor as a clamping device to the protection circuit.

Giving the teaching of Ker'109, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Krakauer in view of Ker'615 by employing the well known or conventional features of providing an ESD protection circuit that efficiently triggers parasitic junction transistor, such as disclosed by Ker, in order to turn on ESD clamp circuits under conditions of ESD overstress.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US Patent No. 5,617,283 and Krakauer hereinafter) in view of Ker et al. (US Pub. No. 2002/0050615 A1 and Ker'615 hereinafter) as applied to claim 1, and further in view of Narita et al. (US Pub. 5,973,901 and Narita hereinafter).

Although the method and apparatus disclosed by Krakauer in view of Ker'615 shows substantial features of the claimed invention (discussed in the paragraph above), it fails to disclose:

The protection circuit, where the clamping device is a thyristor [claim 10];

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Krakauer in view of Ker'615, as evidenced by Narita.

Narita discloses a semiconductor circuit device with high electrostatic breakdown endurance having:

The protection circuit, where the clamping device is a thyristor [claim 10] (Fig. 6; col. 6, lines 50-51) to provide a thyristor as a clamping device to the protection circuit.

Giving the teaching of Narita, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Krakauer in view of Ker'615 by employing the well known or conventional features of providing an ESD protection circuit that efficiently triggers parasitic junction transistor, such as disclosed by Ker, in order to turn on ESD clamp circuits under conditions of ESD overstress.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Sitton whose telephone number is (571) 270-

3828. The examiner can normally be reached on Monday through Friday 8:00 AM- 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Walter Benson can be reached on (571) 272-2227. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nelson Sitton/
Examiner, Art Unit 4158
Dec. 12, 2007

/UYEN-CHAU N LE/
Primary Examiner, Art Unit 4158